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ABSTRACT

A numeric counter oscillator is disclosed comprising a quotient accumulator

15   and a remainder accumulator. The quotient accumulator has a programmable input
for receiving a QUOTIENT value, a reference clock input and a multi-bit output. The
output is adapted for transmitting an output value OUT representing an accumulated
quotient sum. The multi-bit output increments by a predetermined amount in
response to each reference clock period. The remainder accumulator comprises

20   programmable inputs for receiving respective REMAINDER and DIVISOR values, a
a reference clock input and a multi-bit output representing an accumulated digital
remainder sum less than a predefined digital integer. The remainder accumulator
further comprises a comparator having a first input for receiving a programmed
divisor value, and a second input for receiving the remainder accumulator multi-bit

25   output. The comparator is operative to generate an increment carry signal for
application to the quotient accumulator when the remainder multi-bit output reaches
the predefined integer value.